Remarks/Arguments:

Claims 1, 5, 6, 8-16 and 18 were rejected under 35 U.S.C. § 102(b) as anticipated by Matsunaga et al. (U.S. Pub. No. 2001/0013901). Applicants request reconsideration. In particular, Matsunaga does not disclose or suggest:

> ...a bias circuit operable to apply DC voltages directly across the pixels to forward bias the photodiode regions during a step selected from the group consisting of a reset step for each pixel or a charge blanking step for each pixel.

(Emphasis added). Basis for this amendment may be found in the originally filed specification, for example, at page 7, lines 3-5 and FIG. 6. No new matter has been added.

Matsunaga discloses a MOS-type solid state imaging apparatus. In one embodiment, the unit cells do not include reset transistors. Instead, they include address capacitors 69. See Matsunaga FIG. 33 and paragraph 0184. The reset operation is described as follows:

> With the address capacitors 69, the vertical address lines can be addressed without using any vertical selection transistors. After the signal read operation is complete, the signal charge-discharge negative pulses Pd are applied to the vertical address lines 6-1, 6-2 . . . to bias the potentials of the photodiodes 62 to the negative side through the coupling capacitors, thereby discharging the signal charges in the phototiodes to the p-type substrate.

See Matsunga paragraph 0190.

Applicants' claim 1 requires that the bias circuit is operable "to apply voltages directly across the pixels to forward bias the photodiode regions during a step selected from the group consisting of a reset step . . . ." (Emphasis added). Matsunaga, on the other hand, requires that the voltage be applied to the photodiodes "through the coupling capacitors." Thus, Matsunaga does not disclose all features of claim 1.

Applying the voltages directly across the photodiode regions to forward bias the photodiode regions, as opposed to applying the voltages to the photodiode regions through coupling capacitors, enables Applicants' image sensor to forward bias the photodiode regions during a reset operation. During a reset operation, however, the photodiode is reverse-biased. Matsunaga does not describe how they are able to obtain a forward bias on the photodiodes while resetting the photodiodes. We believe it is only possible wherein the application of the voltage to the coupling capacitors produces a signal having generally the following shape.

The negative portion of the signal forward-biases the photodiode and the positive portion of the signal resets the phototiode. Thus, in Matsunaga, the coupling capacitors are necessary parts because they enable generation of a signal that can be used to both forward-bias and reset the photodiode. Applicants, on the other hand, achieves forward-biasing of the photodiode regions during the reset operation without the addition of the coupling capacitors. Accordingly, for the reasons provided above, Applicants' claim 1 is patentable over Matsunaga.

This operation may be disadvantageous as the amount of time the photodiode is forward-biased may not be sufficient to remove the residual charge, as described at page 7, lines 1-8 of the subject application. In addition, the positive peak following the negative peak may not be sufficient to fully reset the pixel, limiting its dynamic range. Thus, the subject invention as defined by claim 1 may represent an advantage over Matsunaga.

Claim 18, while not identical to claim 1, includes features similar to claim 1. Accordingly, claim 18 is also patentable over Matsunaga for the reasons provided above.

Claims 5, 6 and 8-16 include all features of claim 1 from which they depend. Thus, claims 5, 6 and 8-16 are also patentable over Matsunaga for the reasons provided above.

Applicants appreciate the indication in the Office Action that claims 17 and 20 would be allowed if amended to include the limitations of their base claims and any intervening claims. Claim 20 has been so amended and, thus, is in condition for allowance. Claim 17 depends from claims 1 and 10 and is not subject to rejection in view of Matsunaga for at least the same reasons as those claims.

In view of the foregoing amendments and remarks, Applicants request that the Examiner reconsider and withdraw the rejection of claims 1, 5, 6, 8-16 and 18 and the objections to claims 17 and 20.

Respectfully submitted,

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